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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: THOMAS J. SONDERMAN, SCOTT BUSHMAN, CRAIG WILLIAM CHRISTIAN	Group Art Unit: 2813
	Examiner: E. KIELIN
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Serial No.: 09/880,975	
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	CUSTOMER NO.: 23720
For: METHOD AND APPARATUS FOR CONTROLLING A THICKNESS OF A COPPER FILM	

APPEAL BRIEF

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
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Sir:

Appellants hereby submit an original and two copies of this Appeal Brief to the Board of Patent Appeals and Interferences in response to the Final Office Action dated October 25, 2004.

A Notice of Appeal for the above-captioned application was filed on December 29, 2004, and the date stamped by the USPTO Mailroom indicates that it was stamped on January 3, 2005; therefore, the two-month date for filing the Appeal Brief is March 3, 2005. Since this Appeal Brief is being filed on January 28, 2005, it is believed that this Appeal Brief is timely filed. However, if an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also

constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

The Director is authorized to deduct the fee for filing this Appeal Brief ($500.00) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT3258. In the event the monies in that account are insufficient, the Commissioner is authorized to withdraw funds from Williams, Morgan & Amerson, P.C., Deposit Account No. 50-0786/2000.045300/TT3258.

I. REAL PARTY IN INTEREST

The present application is owned by Advanced Micro Devices, Inc.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 2-6, 13-21 and 23-31 were withdrawn from consideration in the response to the Office Action mailed October 25, 2004. Claims 1, 7-12 and 22 are pending in the application. Claims 1, 7-12 and 22 stand rejected under 35 U.S.C. § 103(a), as being made unpatentable by U.S. Patent No. 6,428,673 B1 (***Ritzdorf***) in view of U.S. Patent 6,221,765 B1 (***Ueno***) and U.S. 6,298,470 B1 (***Breiner***). Claims 1, 7, 8, 10, 11, and 22 stand rejected under 35 U.S.C. § 103(a) as being made unpatentable by U.S. Patent No. 6,428,673 B1 (***Ritzdorf***) in view of U.S. Patent No. 6,221,765 B1 (***Ueno***) and U.S. Patent No. 6,211,094 B1 (***Jun***). The claims on appeal (claims 1, 7-12 and 22), as well as the previously withdrawn claims, are set forth in Appendix A.

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections provided in the Final Office Action Dated October 25, 2004.

V. SUMMARY OF THE INVENTION

In general, the present invention is directed towards the manufacture of a semiconductor device. Appellants' inventive methodologies are generally directed to forming a copper layer on a semiconductor device, such as a semiconductor wafer. The inventive methodologies include averaging a plurality of thicknesses from a plurality of locations and comparing the measured thickness to desired thickness. The present patent application also discloses measuring a mechanical stress and varying the thickness based upon the actual thickness differing from the desired thickness and the mechanical stress.

In general, the present invention is directed towards the manufacture of a semiconductor device. As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of technologies, for example, NMOS, PMOS, CMOS, and the like, and is readily applicable to a variety of devices, including, but not limited to, logic devices, memory devices, and the like. (*See*, Specification, page 7, lines 20 to 24).

As shown in Figure 1, a first dielectric layer 120 and a first conductive structure 140 (such as a copper intermetal via connection) may be formed above a structure layer 100 such as a semiconducting substrate. However, the present invention is not limited to the formation of a copper (Cu)-based interconnect above the surface of a semiconducting substrate such as a silicon

wafer, for example. Rather, as will be apparent to one skilled in the art upon a complete reading of the present disclosure, a copper (Cu)-based interconnect formed in accordance with the present invention may be formed above previously formed semiconductor devices and/or process layer, *e.g.*, transistors, or other similar structure. In effect, the present invention may be used to form process layers on top of previously formed process layers. The structure layer 100 may be an underlayer of semiconducting material, such as a silicon substrate or wafer, or, alternatively, may be an underlayer of semiconductor devices, such as a layer of metal oxide semiconductor field effect transistors (MOSFETs), and the like, and/or a metal interconnection layer or layers (see Figure 9, for example) and/or an interlevel (or interlayer) dielectric (ILD) layer or layers, and the like. (*See*, Specification, page 8, lines 1 to 15).

In a single-damascene copper process flow, according to various embodiments of the present invention, as shown in Figures 1-8, the first dielectric layer 120 is formed above the structure layer 100, adjacent the first conductive structure 140. As shown in Figure 1, the first dielectric layer 120 has an etch stop layer (ESL) 110 (typically silicon nitride, Si_3N_4, or SiN, for short) formed and patterned thereon, between the first dielectric layer 120 and a second dielectric layer 130 and adjacent the first conductive structure 140. The second dielectric layer 130 is formed above the etch stop layer (ESL) 110 and above the first conductive structure 140. The first dielectric layer 120 has the first conductive structure 140 disposed therein. If necessary, the second dielectric layer 130 may have been planarized using a chemical-mechanical polishing (CMP) process. The second dielectric layer 130 has an etch stop layer 160 (typically also SiN) formed and patterned thereon, between the second dielectric layer 130 and a patterned photomask 150. The patterned photomask 150 is formed and patterned above the etch stop layer 160. (*See*, Specification, page 8, lines 17 to 25 and page 9, lines 1 to 4).

The first and second dielectric layers 120 and 130 may be formed from a variety of dielectric materials, including, but not limited to, materials having a relatively low dielectric constant (low K materials, where K is less than or equal to about 4), although the dielectric materials need not have low dielectric constants. The first and second dielectric layers 120 and 130 may be formed by a variety of known techniques for forming such layers, *e.g.*, a chemical vapor deposition (CVD) process, a low-pressure CVD (LPCVD) process, a plasma-enhanced CVD (PECVD) process, a sputtering process, a physical vapor deposition (PVD) process, a spin-on coating process (such as a spin-on glass process), and the like, and each may have a thickness ranging from approximately 3000 Å-8000 Å, for example. (*See*, Specification, page 7, lines 20 to 24). (*See*, Specification, page 9, lines 6 to 14).

The first and second dielectric layers 120 and 130 may be formed from a variety of low K dielectric materials, where K is less than or equal to about 4. Examples include Applied Material's Black Diamond®, Novellus' Coral®, Allied Signal's Nanoglass®, JSR's LKD5104, and the like. In one illustrative embodiment, the first and second dielectric layers 120 and 130 are each comprised of Applied Material's Black Diamond®, each having a thickness of approximately 5000 Å, each being formed by being blanket-deposited by an LPCVD process for higher throughput. (*See*, Specification, page 9, lines 16 to 22).

As shown in Figure 2, a metallization pattern is then formed by using a patterned photomask 150, the etch stop layers 160 and 110 (Figures 1-2), and photolithography. For example, openings (such as an opening or trench 220 formed above at least a portion of the first conductive structure 140) for conductive metal lines, contact holes, via holes, and the like, are

etched into the second dielectric layer 130 (Figure 2). The opening 220 has sidewalls 230. The opening 220 may be formed by using a variety of known anisotropic etching techniques, such as a reactive ion etching (RIE) process using hydrogen bromide (HBr) and argon (Ar) as the etchant gases, for example. Alternatively, an RIE process with CHF_3 and Ar as the etchant gases may be used, for example. Plasma etching may also be used in various illustrative embodiments. The etching may stop at the etch stop layer 110 and at the first conductive structure 140. (*See*, Specification, page 9, lines 24 to 25 and page 10, lines 1 to 9).

As shown in Figure 3, the patterned photomask 150 (Figures 1-2) is stripped off, by ashing, for example. Alternatively, the patterned photomask 150 may be stripped using a 1:1 solution of sulfuric acid (H_2SO_4) to hydrogen peroxide (H_2O_2), for example. (*See*, Specification, page 10, lines 11 to 13).

As shown in Figure 4, the etch stop layer 160 is then stripped off, by selective etching, for example. In various illustrative embodiments, for example, in which the etch stop layer 160 comprises silicon nitride (Si_3N_4), hot aqueous phosphoric acid (H_3PO_4) may be used to selectively etch the silicon nitride (Si_3N_4) etch stop layer 160. (*See*, Specification, page 10, lines 15 to 18).

As shown in Figure 5, a thin barrier metal layer 525A and a copper seed layer 525B (or a seed layer of another conductive material) are applied to the entire surface using vapor-phase deposition. The barrier metal layer 525A and the copper (Cu) seed layer 525B blanket-deposit an entire upper surface 530 of the second dielectric layer 130 as well as the side surfaces 230 and a bottom surface 550 of the opening 220, forming a conductive surface 535, as shown in Figure 5. (*See*, Specification, page 10, lines 20 to 25).

The barrier metal layer 525A may be formed of at least one layer of a barrier metal material, such as tantalum (Ta) or tantalum nitride (TaN), and the like, or, alternatively, the barrier metal layer 525A may be formed of multiple layers of such barrier metal materials. For example, the barrier metal layer 525A may also be formed of titanium nitride (TiN), titanium-tungsten, nitrided titanium-tungsten, magnesium, a sandwich barrier metal Ta/TaN/Ta material, or another suitable barrier material. Tantalum nitride (TaN) is believed to be a good diffusion barrier to copper (Cu). Tantalum (Ta) is believed to be easier to deposit than tantalum nitride (TaN), while tantalum nitride (TaN) is easier to subject to a chemical mechanical polishing (CMP) process than tantalum (Ta). The copper seed layer 525B may be formed on top of the one or more barrier metal layers 525A by physical vapor deposition (PVD) or chemical vapor deposition (CVD), for example. (*See*, Specification, page 11, lines 1 to 12).

The bulk of the copper trench-fill is frequently done using an electroplating technique, where the conductive surface 535 is mechanically clamped to an electrode (not shown) to establish an electrical contact, and the structure layer 100 and overlying layers are then immersed in an electrolyte solution containing copper (Cu) ions. An electrical current is then passed through the workpiece-electrolyte system to cause reduction and deposition of copper (Cu) on the conductive surface 535. In addition, an alternating-current bias of the workpiece-electrolyte system has been considered as a method of self-planarizing the deposited copper (Cu) film, similar to the deposit-etch cycling used in high-density plasma (HDP) tetraethyl orthosilicate (TEOS) dielectric depositions. (*See*, Specification, page 11, lines 14 to 22).

As shown in Figure 6, this process typically produces a conformal coating of a copper (Cu) layer 640 of substantially constant thickness across the entire conductive surface 535. The copper (Cu) layer 640 may then be annealed using a rapid thermal anneal (RTA) process

performed at a temperature ranging from approximately 100-400°C for a time ranging from approximately 10-180 seconds. Alternatively, the copper (Cu) layer 640 may be annealed using a furnace anneal process at a temperature ranging from approximately 100-400°C for a time ranging from approximately 10-90 minutes. In various alternative embodiments, the copper (Cu) layer 640 may be annealed using a rapid thermal anneal (RTA) process performed at a temperature ranging from approximately 250-350°C for a time ranging from approximately 10-180 seconds. In still other various illustrative embodiments, the copper (Cu) layer 640 may be annealed using a furnace anneal process at a temperature ranging from approximately 250-350°C for a time ranging from approximately 10-90 minutes. (*See*, Specification, page 11, lines 24 to 25 and page 12, lines 1 to 10).

A post-formation anneal may be used to accelerate room-temperature grain growth in the copper (Cu) layer 640, and, consequently, may affect the mechanical stress state of the copper (Cu) layer 640. In particular, the post-formation anneal of over-filled damascene openings, such as opening 220 shown in Figure 6, affects the mechanical stress state of the copper (Cu) layer 640. For anneals performed at temperatures ranging from about 150-400°C, the copper (Cu) layer 640 is in a relatively low mechanical stress state that is effectively mechanical stress-free, or slightly compressive, since the copper (Cu) has no native oxide strengthening mechanism and since the copper (Cu) grain size is small. The copper (Cu) grain growth in the small-grained copper (Cu) layer 640 under compression will act to relax the mechanical stress. In the copper (Cu) in the opening 220 covered by the sufficiently thick layer of the copper (Cu) layer 640, it is likely that the mechanical stress in the copper (Cu) would be about zero or at least very small at the anneal temperatures ranging from about 150-400°C. The microstructure of the copper (Cu) in the opening 220 is influenced by the sufficiently thick layer of the copper (Cu)

layer 640, and it is believed that the mechanical stress in the copper (Cu) in the opening 220 is also influenced by the sufficiently thick layer of the copper (Cu) layer 640. (*See*, Specification, page 12, lines 12 to 25 and page 13, lines 1 to 2).

Upon cooling from the anneal, the mechanical stress in the copper (Cu) in the opening 220 is tensile. Since the copper (Cu) of the copper (Cu) layer 640 has a thickness, measured from the bottom of the opening 220, in a range of approximately 3000 Å-8000 Å, for example, the mechanical stress in the copper (Cu) in the opening 220 is relatively small, with hydrostatic stresses in a range of from about 50 MPa to about 200 MPa. (*See*, Specification, page 13, lines 4 to 8).

The mechanical stress in the copper (Cu) in the opening 220 is tensile, after cooling down from the anneal, due in part to the difference in the coefficient of thermal expansion (ΔCTE) between the copper (Cu) in the copper (Cu) layer 640 and the semiconducting material of the structure layer 100. For example, the coefficient of thermal expansion (CTE) for silicon (Si) is about 2.6×10^{-6}/°C, the coefficient of thermal expansion (CTE) for copper (Cu) is about 16.6×10^{-6}/°C, and the coefficient of thermal expansion (CTE) for aluminum (Al) is about 23.1×10^{-6}/°C. Therefore, the difference in the coefficient of thermal expansion (ΔCTE) between copper (Cu) and silicon (Si) is about 14.0×10^{-6}/°C. For the sake of comparison, the difference in the coefficient of thermal expansion (ΔCTE) between aluminum (Al) and silicon (Si) is about 20.5×10^{-6}/°C, or about 1.46 times larger than the difference in the coefficient of thermal expansion (ΔCTE) between copper (Cu) and silicon (Si). The difference in the coefficient of thermal expansion (ΔCTE) is the dominant source of mechanical strain in a metallic interconnect. (*See*, Specification, page 13, lines 10 to 22).

The mechanical stress may be calculated from the mechanical strain using mechanical stiffness coefficients. An order of magnitude estimate of the mechanical stress may be calculated using the biaxial modulus. The biaxial modulus of silicon (Si) is about 1.805×10^5 MPa (MegaPascals), the biaxial modulus of copper (Cu) is about 2.262×10^5 MPa, and the biaxial modulus of aluminum (Al) is about 1.143×10^5 MPa, or about half the biaxial modulus of copper (Cu). (*See*, Specification, page 13, lines 24 to 25 and page 14, lines 1 to 4).

In one illustrative embodiment, copper (Cu) lines having critical dimensions of about 0.25 μm, and a thickness of approximately 4500 Å, similar to the copper (Cu) layer 640, are subjected to a post-plating anneal using a furnace anneal process performed at a temperature of approximately 250°C for a time of approximately 30 minutes. The mechanical stresses measured along the lengths (X direction, into the page of Figure 6) of these copper (Cu) lines are about 300 MPa, the mechanical stresses measured along the widths (Y direction, horizontal arrows in Figure 6) of these copper (Cu) lines are about 160 MPa, and the mechanical stresses measured along the heights (Z direction, horizontal arrows in Figure 6) of these copper (Cu) lines are about 55 MPa. The hydrostatic mechanical stress measured with these copper (Cu) lines is about 175 MPa. (*See*, Specification, page 14, lines 6 to 15).

These mechanical stress levels appear to be a function of the post-plating anneal temperature. By way of comparison, copper (Cu) lines having critical dimensions of about 0.25 μm, and a thickness of approximately 4500 Å, similar to the copper (Cu) layer 640, subjected to a post-plating anneal using a furnace anneal process performed at a higher temperature of approximately 500°C for the same time of approximately 30 minutes have been measured to have the following mechanical stresses. The mechanical stresses measured along the

lengths (X direction) of these copper (Cu) lines are about 600 MPa, the mechanical stresses measured along the widths (Y direction) of these copper (Cu) lines are about 470 MPa, and the mechanical stresses measured along the heights (Z direction) of these copper (Cu) lines are about 230 MPa. The hydrostatic mechanical stress measured with these copper (Cu) lines is about 440 MPa. Since hydrostatic mechanical stress is the driving force for void formation in metallic interconnects, efforts should be made to reduce this hydrostatic mechanical stress. Thus, the post-plating anneal temperature should be lowered to reduce this hydrostatic mechanical stress. For example, a post-plating furnace anneal process performed at approximately 250°C for approximately 30 minutes, which produces a hydrostatic mechanical stress of about 175 MPa, is preferable to a post-plating furnace anneal process performed at approximately 500°C for approximately 30 minutes, which produces a hydrostatic mechanical stress of about 440 MPa. (*See*, Specification, page 14, lines 17 to 25 and page 15, lines 1 to 9).

As shown in Figure 7, following the post-deposition anneal described above, the layer of the copper (Cu) layer 640 is planarized using chemical mechanical polishing (CMP) techniques. The planarization using CMP clears all copper (Cu) and barrier metal from the entire upper surface 530 of the second dielectric layer 130, leaving a copper (Cu) portion 740 of the copper (Cu) layer 640 remaining in a metal structure such as a copper (Cu)-filled trench, forming a copper (Cu)-interconnect 745, adjacent remaining portions 725A and 725B of the one or more barrier metal layers 525A and copper seed layer 525B (Figures 5 and 6), respectively, as shown in Figure 7. (*See*, Specification, page 15, lines 11 to 18).

As shown in Figure 7, the copper (Cu)-interconnect 745 may be formed by annealing the copper (Cu) portion 740, adjacent the remaining portions 725A and 725B of the one or more barrier metal layers 525A and copper seed layer 525B (Figures 5 and 6), to the first conductive

structure 140. The anneal process may be performed in a traditional tube furnace, at a temperature ranging from approximately 100-500°C, for a time period ranging from approximately 10-90 minutes, in a nitrogen-containing ambient that may include at least one of ammonia (NH_3), molecular nitrogen (N_2), molecular hydrogen (H_2), argon (Ar), and the like. Alternatively, the anneal process may be a rapid thermal anneal (RTA) process performed at a temperature ranging from approximately 100-500°C for a time ranging from approximately 10-180 seconds in a nitrogen-containing ambient that may include at least one of molecular nitrogen (N_2), molecular hydrogen (H_2), argon (Ar), and the like. (*See*, Specification, page 15, lines 20 to 25 and page 16, lines 1 to 5).

As shown in Figure 8, the second dielectric layer 130 may be planarized, as needed, using chemical mechanical polishing (CMP) techniques. Planarization would leave the planarized second dielectric layer 130 adjacent the copper (Cu)-interconnect 745 and above the etch stop layer 110, forming a copper (Cu)-interconnect layer 800. The copper (Cu)-interconnect layer 800 may include the copper (Cu)-interconnect 745 adjacent the second dielectric layer 130. The copper (Cu)-interconnect layer 800 may also include the etch stop layer 110. As shown in Figure 8, the copper (Cu)-interconnect layer 800 may also include an etch stop layer 820 (also known as a "hard mask" and typically formed of silicon nitride, Si_3N_4, or SiN, for short) formed and patterned above the second dielectric layer 130 and above at least a portion of the copper (Cu)-interconnect 745. (*See*, Specification, page 16, lines 7 to 16).

As shown in Figure 9, the copper (Cu)-interconnect layer 800 may be an underlying structure layer (similar to the structure layer 100) to a copper (Cu)-interconnect layer 900. The copper (Cu)-interconnect layer 900 may include a copper (Cu)-filled trench 940 and an intermetal via connection 910 adjacent a planarized dielectric layer 935. The intermetal via

connection 910 may be a copper (Cu) structure similar to the first copper (Cu) structure 140, and the intermetal via connection 910 may be annealed to the copper (Cu)-filled trench 940 in a similar fashion to the anneal described above in relation to the formation of the copper (Cu)-interconnect 745 (Figure 7). The copper (Cu)-interconnect layer 900 may also include the etch stop layer 820 and/or etch stop layer 915 and/or etch stop layer 920 (also known as "hard masks" and typically formed of silicon nitride, Si_3N_4, or SiN, for short) formed and patterned above the planarized dielectric layers 925 and/or 935, respectively. The etch stop layer 920 may also be formed above at least a portion of the copper (Cu)-filled trench 940. (*See*, Specification, page 16, lines 18 to 25 and page 17, lines 1 to 4).

Turning now to Figure 10, one illustrative embodiment of a system 1000 that may be used to produce the features of the semiconductor device depicted in Figures 1-9 is shown. The system 1000 processes wafers 1002 and is generally comprised of a photolithography tool 1004, a stepper 1006, an etcher 1007, a barrier deposition tool 1008, an electroplate tool 1009, a metrology tool 110, and a controller 1012. The wafer 1002 is generally serially processed within each of the tools 1004-1009, and then analyzed in the metrology tool 1010. Those skilled in the art will appreciate that more or fewer tools may be included in the system 1000 as is warranted to produce the desired features on the wafer 1002. (*See*, Specification, page 17, lines 6 to 13).

Generally, the photolithography tool 1004 forms a layer of photoresist on the wafer 1002. The stepper 1006 controllably exposes the layer of photoresist to a light source through a mask or reticle to produce a desired pattern in the layer of photoresist. The etcher 1007 removes those portions of layers underlying the layer of photoresist that are exposed by the patterning produced by the mask to produce openings and/or holes in a desired pattern. The thin barrier metal layer is deposited by a barrier deposition tool 1008. The electroplate tool 1009 forms a layer or film of

copper on the surface of the wafer 1002, filling the openings and/or holes. The metrology tool 1010 measures select parameters of the wafer 102, such as physical characteristics and/or electrical properties. The measured physical characteristics may include thickness of the copper layer, feature sizes, depth of an etching process, etc. The measured electrical properties may include resistance, conductivity, voltage levels, etc. In some embodiments, the metrology tool 1010 may not be needed, as sufficient feedback information for controlling parameters of the tools 1004-1009 may be obtained from sensors within the tools 1004-1009. (*See*, Specification, page 17, lines 15 to 25 and page 18, lines 1 to 3).

The metrology tool 1010 may be any of a variety of devices used to measure electrical and/or structural features on the wafer 1002 after being processed by the tools 1004-1009. For example, the metrology tool 1010 may be configured to measure feature sizes on the wafer 1002, such as the thickness of the copper layer, and provide the measurement data to the controller 1012. Measurements of this type may be useful in determining whether the electroplating process has produced a layer of copper having a desired thickness, and then modifying the operation of the electroplate tool 1009, if necessary, so that subsequently processed wafers 1002 have the desired thickness. Such a metrology tool is available from Rudolph Technologies as model number 200, Tencor as Model NC110, or the like. It is contemplated that in some embodiments of the instant invention additional tools (not shown) may be deployed in the manufacturing line, such as additional metrology tools 1010 positioned to measure certain mechanical or electrical parameters of the wafer 1002 at various steps in the manufacturing process. Alternatively, additional tools may be deployed intermediate the etcher 1007 and the electroplate tool 1009. These intermediate devices may perform additional processes, such as cleaning, rinsing, forming additional layers, etc. Moreover, it is anticipated that the formation of

some of the features on the wafer 1002 will be produced by operations performed by the tools 1004-1009 other than in the order illustrated. For example, it may be useful to route the wafer 1002 through the photolithography tool 1004, stepper 1006 and etcher 1007 a plurality of times before delivering the wafer 1002 to the electroplate tool 1009. (*See*, Specification, page 18, lines 5 to 24).

The etcher 1007 may be any of a variety of devices capable of removing underlying process layers not protected by the layer of photoresist. For example, an etcher commercially available from Applied Materials as model 5000-DPS may be used. Any of a variety of etchants may be employed without departing from the spirit and scope of the instant invention. In one exemplary embodiment, the etcher 1007 employs plasma etching. (*See*, Specification, page 19, lines 1 to 5).

The controller 1012 of Figure 10 may take a variety of forms. For example, the controller 1012 may be included within the tools 1004-1010, or it may be a separate device electrically coupled to the tools 1004-1010 via lines 1014-1020, respectively. In the embodiment illustrated herein, the controller 1012 takes the form of a computer that is controlled by a variety of software programs. The software programs that directly relate to controlling and or monitoring the electroplate tool 1009 are discussed in greater detail below in conjunction with Figures 12-13. Those of ordinary skill in the art having the benefit of this disclosure will appreciate that the controller 1012 need not rely on software for its functionality, but rather, a hardware controller may be used to provide the functionality described herein and attributed to the controller 1012. Further, the controller 1012 need not be coupled only to the tools 1004-1010, but rather, could be coupled to and involved in controlling or collecting data from other

devices involved in the manufacture of semiconductor devices. (*See*, Specification, page 19, lines 7 to 19).

In the illustrated embodiment, the automatic process controller 1012 is a computer programmed with software to implement the functions described. However, as will be appreciated by those of ordinary skill in the art, a hardware controller (not shown) designed to implement the particular functions may also be used. Moreover, the functions of the controller described herein may be performed by one or more processing units that may or may not be geographically dispersed. Portions of the invention and corresponding detailed description are presented in terms of software, or algorithms and symbolic representations of operations on data bits within a computer memory. These descriptions and representations are the ones by which those of ordinary skill in the art effectively convey the substance of their work to others of ordinary skill in the art. An algorithm, as the term is used here, and as it is used generally, is conceived to be a self-consistent sequence of steps leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of optical, electrical, or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, or the like. (*See*, Specification, page 19, lines 21 to 25 and page 20, lines 1 to 11).

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise, or as is apparent from the discussion, terms such as "processing" or "computing" or "calculating" or "determining" or "displaying" or

the like, refer to the actions and processes of a computer system, or similar electronic computing device, that manipulates and transforms data represented as physical, electronic quantities within the computer system's registers and memories into other data similarly represented as physical quantities within the computer system memories or registers or other such information storage, transmission or display devices. (*See*, Specification, page 20, lines 13 to 21).

An exemplary software system capable of being adapted to perform the functions of the automatic process controller 1012, as described, is the KLA Tencor Catalyst system offered by KLA Tencor, Inc. The KLA Tencor Catalyst system uses Semiconductor Equipment and Materials International (SEMI) Computer Integrated Manufacturing (CIM) Framework compliant system technologies, and is based on the Advanced Process Control (APC) Framework. CIM (SEMI E81-0699 - Provisional Specification for CIM Framework Domain Architecture) and APC (SEMI E93-0999 - Provisional Specification for CIM Framework Advanced Process Control Component) specifications are publicly available from SEMI. (*See*, Specification, page 20, lines 23 to 25 and page 21, lines 1 to 6).

Turning now to Figure 11, a stylized representation of the electroplater tool 1009 is shown. Generally, a tank 1100 contains a bath 1102. The wafer 1002 is immersed in the bath 1102 and coupled to electrical ground. Typically, the bath is composed of a salt of the metal to be plated. Thus, in the illustrated embodiment, the bath 1102 is a solution containing a copper salt, such as copper chloride, copper sulfate, or the like. A copper anode 1104 is also immersed in the bath 1102, and is coupled to receive an electrical signal from a controller 1106 over a line 1108. Thus, electricity flows from the copper anode to the grounded wafer 1002, transporting copper atoms from the anode 1104 to the bath 1102, and from the bath 1102 to the surface of the wafer 1002. The process continues for a preselected period of time to produce a conformal layer

or film of copper similar to the layer 640 illustrated in Figure 6. The electroplate tool 1009 may be any of a variety of devices capable of depositing a layer of copper on a semiconductor wafer. For example, an electroplate tool commercially available from Semitool as model LT-210t, Novellus as the Sabre model, or the like may be used. (*See*, Specification, page 21, lines 8 to 21).

The thickness of the copper layer 640 may be controlled by altering a variety of parameters. First, the duration that the wafer 1002 remains in the electrolytic solution 1102 with current passing from the anode 1104 to the wafer 1002 will directly impact the thickness of the copper layer 140. That is, reducing the period of time will reduce the thickness of the copper layer 640, and increasing the period of time will increase the thickness of the copper layer. The rate at which the thickness of the copper layer increases may not be constant, but rather, may vary over time, depending upon the condition of the anode 1104 and the bath 1102. Moreover, the type of features present on the wafer 1002 may also impact the rate. For example, increasing the number of features may produce a greater surface area, which may impact the rate at which the thickness of the copper layer 640 increases. (*See*, Specification, page 21, lines 23 to 25 and page 22, lines 1 to 7).

Varying the voltage and/or current applied to the anode 1104 may also impact the rate at which the thickness of the copper layer 640 increases. For example, increasing the voltage/current may raise the rate at which copper is deposited on the wafer 1002. Conversely, lowering the voltage/current may reduce the rate at which copper is deposited on the wafer 1002. Generally, maintaining the voltage applied to the copper anode 1104 in the range of about 2 to 4 volts produces acceptable electroplating characteristics. (*See*, Specification, page 22, lines 9 to 14).

Additionally, the controller 1106 may be configured to provide an AC signal. Varying the frequency, magnitude, and/or shape of the AC signal may also also impact the rate at which the thickness of the copper layer 640 increases. For example, increasing the current may raise the rate at which copper is deposited on the wafer 1002. Conversely, lowering the current may reduce the rate at which copper is deposited on the wafer 1002. Generally, maintaining the current applied to the copper anode 1104 in the range of about 1 to 10 milliamps produces acceptable electroplating characteristics. (*See*, Specification, page 22, lines 16 to 22).

The controller 1106 of the electroplate tool 1019 is coupled to the controller 1012 over the line 1019. This connection allows the controller 1012 to deliver signals that instruct the controller 1106 to vary some or all of the parameters discussed above to alter the thickness of the copper layer 640 based on data received from the metrology tool 1010. For example, if the metrology tool 1010 detects that the copper layer 640 is too thin, then the controller 1012 delivers a control signal to the controller 1106, instructing the controller 1106 to alter one or more of its parameters to increase the thickness of the copper layer 640. (*See*, Specification, page 22, lines 24 to 25 and page 23, lines 1 to 5).

Referring to Figure 12, one illustrative embodiment of a process 1200 used to produce features of the type depicted in Figures 1-9 is generally shown in flowchart form. As shown therein, the present invention comprises the process 1200 beginning at block 1202 where a process layer is formed on the wafer 1200. Thereafter, a layer of photoresist is formed above the process layer, as indicated at block 1204. The method further comprises patterning the layer of photoresist, as indicated at block 1206, and etching away select portions of the underlying process layer, as indicated at block 1208. In block 1210, a layer of copper is formed on the surface of the process layer and in the openings created by the etching process. Thereafter, in

block 1212, the wafer 1002 is analyzed to determine the thickness of the copper layer. The controller 1012 uses the thickness measurement to vary the parameters of the copper forming process so as to increase/decrease the thickness of subsequently formed copper layers, as needed. (*See*, Specification, page 23, lines 7 to 18).

Turning now to Figure 13, a flowchart depiction of a process 1300 used to vary the parameters of the electroplate tool 1009, as identified in the block 1212, is shown. The process 1300 begins at block 1302 with the metrology tool 1010 measuring the thickness of the copper layer 640. The thickness of the copper layer 640 may be determined using a variety of processes. For example, a single measurement may be taken. Alternatively, a plurality of measurements may be made at preselected spaced apart locations on the surface of the wafer 1002. Where a plurality of measurements are made, a criteria may be established for determining the thickness of the layer 640. The criteria may involve averaging the measurements, determining the median value, using the worst case measurement, using the best case measurement, using a ruling majority of measurements, etc. In block 1302, the selected criteria is applied to the measurements to determine the actual thickness of the copper layer 640. (*See*, Specification, page 23, lines 20 to 25 and page 24, lines 1 to 6).

In block 1304, the actual thickness of the copper layer 640 is compared to a desired thickness. As long as the two measurements are within acceptable limits of one another, no action is taken to vary the parameters of the electroplate tool 1009. Where the comparison of the measurements is outside a desired range, the magnitude of the difference is recorded along with an indication of whether the actual thickness is greater or less than the desired thickness. (*See*, Specification, page 24, lines 8 to 13).

In an alternative embodiment, where a plurality of spatially separated measurements of the thickness of the copper layer 640 are made, it may be useful to compare each of these measurements to a desired thickness. In this embodiment, the desired thickness may be the same for each measurement, or it may vary. That is, a desired thickness at position A on the wafer 1002 may be greater or less than a desired thickness at position B. (*See*, Specification, page 24, lines 15 to 19).

In block 1306, the process 1300 determines a desired parameter for the electroplate tool 1009 so as to produce the desired thickness of the copper layer 640. Determining the desired parameter may be accomplished by a formula and/or a lookup table. The values stored in the lookup table and/or the formula may be derived theoretically, or may be determined empirically. That is, a formula that correlates the thickness of the copper layer with parameters, such as time, voltage, current, waveshape, frequency, etc. may be used to calculate the desired setting for the electroplate tool 1009. Alternatively, a series of test runs at a variety of times, voltages, currents, waveshapes, frequencies, etc. may be performed to determine an actual thickness of the copper layer 640 at a variety of these parameters. These empirically determined parameters may then be stored in a lookup table and accessed by the process 1300. Alternatively, the desired parameter of the electroplate tool 1009 may be iteratively adjusted until a desired thickness for the copper layer 640 is observed by the metrology tool 1010. That is, each time a wafer 102 is processed by the electroplate tool 1009 and measured by the metrology tool 1010, the desired parameter may be iteratively adjusted by an amount proportional to the difference between the desired and actual thickness. That is, the greater the difference in thickness, the greater the correction to the desired parameter. (*See*, Specification, page 24, lines 21 to 25 and page 25, lines 1 to 12).

Finally, in block 1308, the desired parameter is communicated to the electroplate tool 1009. The controller 1106 in the electroplate tool 1009 responds by varying the parameter to its new, desired setting for subsequently processed wafers 1002. (*See*, Specification, page 25, lines 14 to 16).

Of course, the present invention should not be considered as limited to the specifically disclosed embodiments discussed immediately above.

VI. ISSUES ON APPEAL

1. Whether or not claims 1, 7-12 and 22 are made unpatentable by U.S. Patent No. 6,428,673 (***Ritzdorf***) in view of U.S. Patent 6,221,765 (***Ueno***) and U.S. 6,298,470 (***Breiner***), pursuant to 35 U.S.C. § 103(a).

2. Whether or not claims 1, 7, 8, 10, 11, and 22 are made unpatentable by U.S. Patent No. 6,428,673 (***Ritzdorf***) in view of U.S. Patent 6,221,765 (***Ueno***) and U6,211,094 (***Jun***), pursuant to 35 U.S.C. § 103(a).

VII. GROUPING OF THE CLAIMS

Claims 1 and 22 are grouped together (Group I), and stand or fall together; claims 7-9, are grouped together (Group II), and stand or fall together; and claims 10-12 are grouped together (Group III), and stand or fall together.

VIII. ARGUMENT

As described above, the present invention provides for forming a copper layer on a semiconductor device, such as a semiconductor wafer. The present invention also provides for

averaging a plurality of thicknesses from a plurality of locations and comparing the measured thickness to desired thickness. The present patent application also discloses measuring a mechanical stress and varying the thickness based upon the actual thickness differing from the desired thickness and the mechanical stress.

The Examiner relies heavily on U.S. Patent No. 6,428,673 (***Ritzdorf***), which discloses that a metrology system can feed forward or feed back uniformity and thickness data to drive a process recipe for electroplating reactors. However, Appellants respectfully assert that ***Ritzdorf*** does not disclose forming an opening upon a first dielectric layer that is formed above a structure upon which the copper layer is formed and controlling a parameter based upon a measured thickness, as called for by claims of the present invention. Also, ***Ritzdorf*** does not disclose averaging the thickness from a plurality of sites on a copper layer as called for by claims of the present invention.

Additionally, the Examiner also relies on U.S. Patent No. 6,221,765 (***Ueno***), which provides the disclosure of residual tensile stress being present on a plating film. However, contrary to the Examiner's arguments, ***Ueno*** does not show why knowing the specific quantity of stress in a copper layer is important, ***Ueno*** merely points out that residual tensile stress may be present and makes a guess that the stress may be the result of shrinking of a plating film.

Furthermore, the Examiner also relies on U.S. Patent No. 6,298,470 (***Breiner***), which is directed to extrapolating known data to a new technology to determine and improve yields. ***Breiner*** discloses using data relating to previous generation IC manufacturing technology and applying them to new generation IC manufacturing technology (see for example, col. 2, lines 54-65, col. 13, lines 44-56). Although ***Breiner*** makes a passing reference to a "mean" value of data

points, as described above, ***Breiner*** does not disclose or make obvious varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness and mechanical stress, as called for by claims of the present invention. Contrary to the Examiner's arguments, the disclosure of multiple measurements for each data point in ***Breiner*** does not refer to averaging a plurality of thicknesses from a plurality of locations on a copper layer, as called for by claims of the present invention.

Furthermore, the Examiner also relies on U.S. Patent Patent No. 6,211,094 (***Jun***), which merely discloses measurement of wafers that are analyzed for thickness at various zones. Appellants respectfully assert that ***Jun*** does not disclose averaging the plurality of thicknesses, and called for by claims of the present invention. Further, ***Jun*** does not disclose comparing the actual thickness to a desired thickness, nor does it disclose measuring a mechanical thickness, as called for by claims of the present invention.

Therefore, the Examiner's erroneous combination of ***Ritzdorf***, ***Ueno***, ***Breiner*** and the erroneous combination of ***Ritzdorf***, ***Ueno***, ***Jun***, do not teach, suggest, or make obvious all of Group I, II and III claims of the present invention.

The specific claims of the present invention are discussed below.

A. **Claims 1, 7-12 and 22 are not anticipated or made obvious by U.S. Patent No. 6,428,673 (*Ritzdorf*) in view of U.S. Patent No. 6,221,765 (*Ueno*) and U.S. Patent No. 6,298,470 (*Breiner*) pursuant to 35 U.S.C. § 103(a).**

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation, either in the references themselves or in

the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is non-obvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142. Appellants respectfully assert that the Examiner did not meet the legal standards to reject claims 8 and 33 under 35 U.S.C. § 103(a), including

because of the fact that the prior art references (***Ritzdorf***, ***Ueno***, and ***Breiner***) does not teach or suggest all the claim limitations of claims 1, 7-12, and 22.

Groups I, II, and III (Claims [1 & 22], [7-9], and [10-12], respectively)

In the Final Office Action Dated October 25, 2004, the Examiner rejected claims 1, 7-12, and 22, under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,428,673 (***Ritzdorf***) in view of U.S. Patent No. 6,221,765 (***Ueno***) and U.S. Patent No. 6,298,470 (***Breiner***). Appellants respectfully assert that the Examiner erred in rejecting claims 1, 7-12, and 22, and assert that these claims are allowable.

Ritzdorf discloses that a metrology system can feed forward or feed back uniformity and thickness data to drive a process recipe for electroplating reactors. However, ***Ritzdorf*** does not disclose averaging the thickness from a plurality of sites on a copper layer. Also, contrary to the Examiner's arguments, ***Ueno*** does not show why knowing the specific quantity of stress in a copper layer is important, ***Ueno*** merely points out that residual tensile stress may be present and makes a guess that the stress may be the result of shrinking of a plating film. Further, the disclosure of multiple measurements for each data point in ***Breiner*** does not refer to averaging a plurality of thicknesses from a plurality of locations on a copper layer, as called for by claims of the present invention. The combination of ***Ritzdorf***, ***Ueno***, ***Breiner*** do not disclose or make obvious all of the elements of claims 1, 7-12, and 22 of the present invention.

In the Final Office Action Dated October 25, 2004, the Examiner stated that Appellants ignored ***Ritzdorf's*** (U.S. Patent No. 6,428,673) use of metrology to control copper deposition. *See*, Final Office Action Dated October 25, 2004, page 9. Appellants respectfully assert that

Appellants did not ignore any aspect of ***Ritzdorf***, instead Appellants merely pointed out that ***Ritzdorf*** does not disclose forming an opening upon a first dielectric layer that is formed above a structure upon which the copper layer is formed and controlling a parameter based upon a measured thickness, as called for by claims of the present invention. Also, Appellants have pointed out that ***Ritzdorf*** does not disclose averaging the thickness from a plurality of sites on a copper layer as called for by claims of the present invention. ***Ritzdorf*** discloses that a metrology system can feed forward or feed back uniformity and thickness data to drive a process recipe for electroplating reactors. *See*, col. 4, lines 38-41. However, this neither reads upon forming an opening upon a first dielectric layer that is formed above a structure upon which the copper layer is formed and controlling a parameter based upon a measured thickness; nor does it read upon averaging the thickness from a plurality of sites on a copper layer, as called for by claims of the present invention. Additionally, as described in further details herein, other art cited by the Examiner does not provide disclosure sufficient to make obvious all of the elements of the claims of the present invention that are not disclosed or suggested by ***Ritzdorf***.

In the Final Office Action Dated October 25, 2004, the Examiner stated that Appellants are attempting to show non-obviousness by attacking references individually. Appellants respectfully disagree. Appellants are not interested in attacking the prior art references individually; Appellants merely pointed to various deficits of the prior art references that are not made up for by the primary reference (***Ritzdorf***). The Examiner attempted to piece together an obviousness argument by extracting various disclosures from three separate prior art references. Appellants merely pointed out that these references have various individual deficits of subject matter, that when combined, all of the elements of claims of the present invention would not be made obvious.

Regarding U.S. Patent No. 6,221,765 (***Ueno***), in the Final Office Action Dated October 25, 2004, the Examiner stated that Appellants distorted the rejection by stating that ***Ueno*** does not disclose modifying a parameter by measuring a stress, which is an element that the Examiner uses ***Ueno*** to provide. *See*, Final Office Action Dated October 25, 2004, page 10. Then, the Examiner stated that ***Ueno*** is provided for showing why knowing the specific quantity of stress is important, which would lead one of ordinary skill in the art, based upon disclosure in ***Ritzdorf***, to make obvious the element of "measuring a stress." Therefore, this amounts to using ***Ueno*** in combination with ***Ritzdorf*** to make obvious the element of "measuring a stress." Accordingly, Appellants are still correct in stating that the Examiner is using ***Ueno*** (in combination with ***Ritzdorf***) to provide the missing element of "measuring a stress". Hence, Appellants respectfully assert that Appellants did not distort the rejection provided.

Contrary to the Examiner's assertion (in the Final Office Action Dated October 25, 2004), ***Ueno*** does not show why knowing the specific quantity of stress in a copper layer is important, ***Ueno*** merely points out that residual tensile stress may be present and makes a guess that the stress may be the result of shrinking of a plating film. *See*, col. 3, lines 33-37. Simply because ***Ueno*** describes a guess as to why residual tensile stress is present and because ***Ritzdorf*** discloses "other parameters" being measured, it does not follow that cited prior art provides sufficient motivation to one of ordinary skill in the art to measure a stress parameter (along with other elements of claims of the present invention). Therefore, Appellants' argument that ***Ueno*** does not provide sufficient motivation or incentive to make obvious the element of "measuring a stress" still holds true. Furthermore, Appellants submit that one skilled in the art would not make obvious the element of "measuring a stress" in the context of claims of the present invention simply because ***Ueno*** merely discloses that tensile stress may occur as a result of

shrinkage of plating film, and simply because ***Ritzdorf*** merely discloses film thickness along with "other measurements"; the combination of which does not make obvious varying a parameter in response to thickness differing from desired thickness and mechanical stress. There is no evidence presented to the contrary. Additionally, even if ***Ritzdorf*** and ***Ueno*** were combined with ***Breiner***, this element of the present invention would still not be made obvious.

Regarding ***Breiner***, in the Final Office Action Dated October 25, 2004, the Examiner asserts that Appellants' arguments regarding ***Breiner*** are based upon a false premise. *See*, page 10 of the Final Office Action Dated October 25, 2004. Appellants respectfully disagree. The Examiner makes this assertion by agreeing with Appellants that the number of points referenced in ***Breiner*** refers to the number of positions in the fabrication process, and not to the number of points on the semiconductor wafer itself; and adds that ***Breiner*** also states that the data may include multiple measurements of each point. However, Appellants respectfully assert that this disclosure in ***Breiner*** does not contradict Appellants' contentions. The disclosure of multiple measurements for each data point in ***Breiner*** does not refer to averaging a plurality of thicknesses from a plurality of locations on a copper layer, as called for by claims of the present invention (see Col. 4, lines 62-63); instead, it refers to more than one measurement of "each data point". This disclosure in ***Breiner*** is preceded by a phrase that supports Appellants' argument. The term "mean value" is put into context by the preceding phrase "multiple measurements for each data point," which suggests a mean or median value for the multiple measurements for each data point and <u>not</u> to the same measurements of different data points [emphasis added] (see, col. 4, lines 61-65). Hence, ***Breiner***, along with the cited prior art, does not make obvious the element of averaging a plurality of thicknesses from a plurality of locations on a copper layer, as called for by claims of the present invention.

Additionally, in the Final Office Action Dated October 25, 2004, the Examiner stated that Appellants' description of the term "wafer map" is based upon a false premise. *See*, page 11 of the Final Office Action Dated October 25, 2004. Appellants respectfully disagree. When reading the disclosure of ***Breiner*** in proper context, the term "wafer map" in ***Breiner*** indeed refers to a reference electrical testing, and the Examiner does not offer any evidence to the contrary. The term "wafer map" is *specifically separated* to discuss electrical testing and refers to electrical test characteristics, such as breakdown voltages, leakage currents, resistivity, *etc.*, (emphasis added). ***Breiner*** discloses using such data to provide a wafer map relating to electrical responses related to the geography of the semiconductor wafer (see item numbers 8 and 9 on col. 4, lines 48-59). There is no evidence in any of the cited prior art references to suggest or make obvious a wafer map relating to the thickness across various portions of the semiconductor wafer. These arguments are provided in more detail below.

Appellants respectfully assert that ***Ritzdorf*** in combination with ***Ueno*** and ***Breiner*** does not disclose or make obvious all of the elements of claim 1 of the present invention. ***Ritzdorf*** does not teach, disclose, or make obvious, all of the elements of claim 1, 7-12, and 22. ***Ritzdorf*** is directed towards a system for receiving a wafer for processing, *e.g.*, electrical chemical plating. ***Ritzdorf*** discloses forming a seed layer upon a wafer and transporting the wafer for further analysis or processing. *See,* col. 9, lines 52-55, col. 10, lines 14-16. However, ***Ritzdorf*** does not disclose forming an opening upon a first dielectric layer that is formed above a structure upon which the copper layer is formed and controlling a parameter based upon a measured thickness as called for by independent claims 1 and 22 of the present invention.

Furthermore, ***Ritzdorf*** does not disclose averaging the thickness from a plurality of sites on a copper layer as called for by claims 1 and 22 of the present invention. Controlling a parameter in response to the thickness data that is averaged from data relating to a plurality of positions are not taught by ***Ritzdorf*** and this deficit is not made up for by ***Ueno*** and/or ***Breiner***. Additionally, neither ***Ritzdorf***, ***Ueno***, nor ***Breiner*** disclose measuring a mechanical stress relating to the first copper layer and varying a parameter to form the first copper layer in response to the actual thickness differing from the desired thickness and the mechanical stress.

The Examiner cites ***Ueno*** to disclose the mechanical stress element of claims 1 and 22. However, ***Ueno*** merely discloses a compressive stress being generated in a film to allow a stress to act in a direction enhancing shrinkage of the plating film. *See,* col. 3, lines 33-37. The plating film disclosed in ***Ueno*** is formed while distorting the semiconductor substrate into a concave. *See,* col. 3, lines 37-39. Therefore, the plating film, in which the compressive stress is generated, is formed in an attempt to prevent void generation. *See,* col. 3, lines 39-47. However, measuring the mechanical stress of a copper layer to modify a parameter used to form the copper layer is not disclosed by ***Ueno***. The compression stress applied by ***Ueno*** is merely performed to prevent void generation. The Examiner uses ***Ueno*** to disclose the missing element of modifying a parameter by measuring a stress, which is indeed not provided by ***Ueno***.

Ueno is merely directed to distorting the semiconductor substrate into a concave to introduce compressive stress to prevent void generation. Therefore, one skilled in the art would not combine the disclosure of ***Ueno*** with ***Ritzdorf*** to call for or make obvious the element of measuring the mechanical stress and varying the parameter based upon the actual thickness differing from the desired thickness and the mechanical stress as called for by claims 1 and 22 of

the present invention. Furthermore, even with the combination of ***Ueno***, elements other than measuring the mechanical stress are missing from the combination of ***Ueno*** with ***Ritzdorf***, and ***Breiner*** does not make up for this deficit, as described below.

Appellants respectfully assert that the term "multiple measurements for each data point," in ***Breiner***, as used by the Examiner, does not refer to a plurality of measurements at different points on a semiconductor wafer. The evidence and reasoning for support of this assertion is provided below. When examining this phrase, one skilled in the art would not ignore the disclosure in ***Breiner*** that actually sheds light to this phrase. As disclosed in ***Breiner***, the "number of points" reference in ***Breiner*** refers to the number of positions in the fabrication process, not the number of points on the semiconductor wafer itself (the evidence for supporting this statement is in col. 4, lines 14-15). Additionally, the term "wafer map" is specifically separated to discuss electrical testing and refers to electrical test characteristics, such as breakdown voltages, leakage currents, resistivity, *etc.* ***Breiner*** discloses using such data to provide a wafer map relating to electrical responses related to the geography of the semiconductor wafer (see item numbers 8 and 9 on col. 4, lines 48-59). Nothing in ***Breiner***, or in the other cited prior art, suggests a wafer map relating to the thickness across various portions of the semiconductor wafer.

Although ***Breiner*** discloses wafer thickness, ***Breiner*** actually points to using wafer maps for electrical testing. ***Breiner*** intentionally omits the discussion of wafer maps when discussing other types of data, such as deposition data, etch data, photolithography data, CMP data, and implant data (see items listed on col. 4, lines 18-59). In a parallel list that discusses various types of data, ***Breiner*** intentionally leaves out the term "wafer map" when discussing all items, except

for discussions of the electrical test. Therefore, ***Breiner*** actually suggests only using wafer maps for electrical type data. Therefore, ***Breiner*** actually teaches away from the claimed invention.

Additionally, ***Breiner*** only provides a passing reference to a "mean" value of data points, as described above, ***Breiner*** does not disclose measuring the thickness of copper layers at a plurality of locations on the copper layer and averaging the resultant data, as called for by the claims of the present invention. Again, the term "mean value" is put into context by the preceding term "multiple measurements for each data point," which suggests a mean or median value for the multiple measurements for each data point and not to the same measurements of different data points (see, col. 4, lines 61-65). Furthermore, claims 1 and 22 (Group I claims) also call for measuring a mechanical stress and modifying a parameter relating to forming a copper layer, which is not disclosed or made obvious by the cited prior art. Support for these amendments may be found in the specification, for example, see page 12 of the specification. Therefore, ***Breiner*** clearly does not disclose or make obvious all of the elements of the claimed invention. Accordingly, combining ***Ritzdorf***, ***Ueno,*** and ***Breiner***, still would not make obvious all of the elements of claims 1 and 22 of the present invention. Therefore, for at least the reasons cited above, claims 1 and 22 (Group I claims) are allowable.

Independent claims 1 and 22, are allowable for at least the reasons cited above. Additionally, dependent claims 7-9 (Group II claims) and claims 10-12 (Group III claims), which depend from independent claim 1, are also allowable for at least the reasons cited above.

B. **Claims 1, 7, 8, 10, 11, and 22 are not anticipated or made obvious by U.S. Patent No. 6,428,673 (*Ritzdorf*) in view of U.S. Patent No. 6,221,765 (*Ueno*) and U.S. Patent No. 6,211,094 (*Jun*) pursuant to 35 U.S.C. § 103(a).**

Groups I, II, and III (Claims [1 & 22], [7-9], and [10-12], respectively)

Appellants respectfully assert that the Examiner did not meet the legal standards (described in Part A of this section) to reject claims 1, 7, 8, 10, 11, and 22 under 35 U.S.C. § 103(a), including because of the fact that the prior art references (***Ritzdorf***, ***Ueno***, and ***Jun***) does not teach or suggest all the claim limitations of claims 1, 7-12, and 22.

In the Final Office Action Dated October 25, 2004, the Examiner rejected claims 1, 7, 8, 10, 11, and 22, under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,428,673 (***Ritzdorf***) in view of U.S. Patent No. 6,221,765 (***Ueno***) and U.S. Patent No. 6,211,094 (***Jun***). Appellants respectfully traverse this rejection. Appellants respectfully assert that the Examiner erred in rejecting claims 1, 7, 8, 10, 11, and 22, and assert that these claims are allowable.

The Examiner combines ***Ritzdorf*** and ***Ueno*** with ***Jun*** to reject claims 1, 7, 8, 10, 11, and 22; however, Appellants respectfully traverse this rejection. As described above, ***Ritzdorf*** does not disclose all of the elements of claims 1 and 22 of the present invention and the disclosure of ***Ueno*** and ***Jun*** would still not make up for this deficit. For example, as described above, ***Ritzdorf*** does not teach the averaging element or measuring of the mechanical stress to modify a parameter. The compressive stress disclosed by ***Ueno*** still does not make up for this deficit, as described above. Additionally, the Examiner cites ***Jun*** to assert obviousness of the element of averaging the plurality of thickness to form a plurality of locations. However, ***Jun*** merely discloses measurement of wafers that are analyzed for thickness at various zones. Appellants

respectfully assert that ***Jun*** does not disclose averaging the plurality of thicknesses from a plurality of locations on the copper layer, as called for by claims 1 and 22 (Group I claims) of the present invention. ***Jun*** does not disclose comparing the actual thickness to a desired thickness as called for by claims 1 and 22 of the present invention. Furthermore, ***Jun*** does not disclose measuring the mechanical stress relating to a copper layer and, as described above, this element is not disclosed or made obvious by ***Ritzdorf*** or ***Ueno.*** Therefore, adding the disclosure of ***Jun*** to ***Ritzdorf*** and/or ***Ueno*** still would not disclose or make obvious all of the elements of claims 1 and 22 (Group I claims) of the present invention. Therefore, claims 1, 7, 8, 10, 11, and 22, are not disclosed or made obvious by ***Ritzdorf, Jun***, ***Ueno*** or their combination, for at least the reasons described above. Therefore, claims 1 and 22 (Group I claims), 7-9 (Group II claims), and 10-12 (Group III claims), are allowable for at least the reasons cited above.

Independent claims 1 and 22, are allowable for at least the reasons cited above. Additionally, dependent claims 7-9 (Group II claims) and claims 10-12 (Group III claims), which depend from independent claim 1, are also allowable for at least the reasons cited above.

In light of the arguments presented above, Appellants respectfully assert that claims 1, 7-12 and 22 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

IX. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1, 7-12 and 22, over the prior art of record. In view of the foregoing remarks, Appellants respectfully request that the Board of

Patent Appeals and Interferences reverse the decision rejecting claims 1-22, and direct the Examiner to pass the case to issue.

The undersigned attorney may be contacted at (713) 934-4069 with respect to any questions, comments, or suggestions relating to this appeal.

Date: February 28, 2005	Respectfully submitted, WILLIAMS, MORGAN & AMERSON, P.C. CUSTOMER NO. 23720 By: _____ Jaison C. John, Reg. No. 50,737 10333 Richmond, Suite 1100 Houston, Texas 77042 (713) 934-7000 (713) 934-7011 (facsimile) ATTORNEY FOR APPELLANTS

APPENDIX A

1. (Previously Presented) A method comprising:

forming a first dielectric layer above a first structure layer;

forming a first opening in the first dielectric layer;

forming a first copper layer above the first dielectric layer and in the first opening; and

measuring an actual thickness of the copper layer, measuring the actual thickness comprises averaging a plurality of thicknesses from a plurality of locations on said first copper layer;

comparing the actual thickness to a desired thickness;

measuring a mechanical stress relating to said first copper layer;

varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness and said mechanical stress.

2. (Withdrawn) The method of claim 1, wherein forming the first dielectric layer comprises forming the first dielectric layer using a dielectric material having a dielectric constant K of at most about four, and forming the first dielectric layer using at least one of a chemical vapor deposition (CVD) process, a low pressure CVD (LPCVD) process, a plasma enhanced CVD (PECVD) process, a sputtering process, a physical vapor deposition (PVD) process, and a spin on coating process.

3. (Withdrawn) The method of claim 1, wherein forming the first opening in the first dielectric layer comprises forming the first opening in the first dielectric layer using one of a

mask of photoresist and an etch stop layer, the one of the mask of photoresist and the etch stop layer being formed and patterned above the first dielectric layer.

4. (Withdrawn) The method of claim 3, wherein using the one of the mask of photoresist and the etch stop layer comprises using the etch stop layer being formed of silicon nitride.

5. (Withdrawn) The method of claim 1, wherein forming the copper layer comprises forming the copper layer using electrochemical deposition of copper.

6. (Withdrawn) The method of claim 5, wherein using the electrochemical deposition of the copper comprises forming at least one barrier layer and a copper seed layer in the first opening before the electrochemical deposition of the copper.

7. (Original) The method of claim 1, wherein measuring the actual thickness of the copper layer further comprises measuring the actual thickness of the copper layer at a plurality of locations.

8. (Original) The method of claim 7, wherein measuring the actual thickness of the copper layer at a plurality of locations further comprises averaging the plurality of measurements of the actual thickness.

9. (Original) The method of claim 7, wherein measuring the actual thickness of the copper layer at a plurality of locations further comprises selecting a median measurement as the actual thickness.

10. (Original) The method of claim 7, wherein comparing the actual thickness to the desired thickness further comprises comparing the desired thickness to each of the plurality of measured thickness.

11. (Original) The method of claim 8, wherein comparing the actual thickness to the desired thickness further comprises comparing the desired thickness to the averaged measured thickness.

12. (Original) The method of claim 9, wherein comparing the actual thickness to the desired thickness further comprises comparing the desired thickness to the median thickness.

13. (Withdrawn) The method of claim 1, wherein forming the first copper layer further comprises electroplating the first copper layer above the first dielectric layer and in the first opening.

14. (Withdrawn) The method of claim 13, wherein varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness further comprises varying an amount of time that the first copper layer is electroplated above the first dielectric layer and in the first opening.

15. (Withdrawn) The method of claim 14, wherein varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness further comprises increasing the amount of time that the first copper layer is electroplated above the first dielectric layer and in the first opening in response to the desired thickness being greater than the actual thickness.

16. (Withdrawn) The method of claim 14, wherein varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness further comprises decreasing the amount of time that the first copper layer is electroplated above the first dielectric layer and in the first opening in response to the desired thickness being less than the actual thickness.

17. (Withdrawn) The method of claim 13, wherein varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness further comprises varying at least one of a current and voltage applied to an anode while electroplating the layer of copper above the first dielectric layer and in the first opening.

18. (Withdrawn) The method of claim 17, wherein varying at least one of a current and voltage further comprises increasing at least one of the current and voltage while the first copper layer is electroplated above the first dielectric layer and in the first opening in response to the desired thickness being greater than the actual thickness.

19. (Withdrawn) The method of claim 17, wherein varying at least one of a current and voltage further comprises decreasing at least one of the current and voltage while the first copper layer is electroplated above the first dielectric layer and in the first opening in response to the desired thickness being less than the actual thickness.

20. (Withdrawn) The method of claim 17, wherein varying at least one of the current and voltage further comprises varying the frequency of at least one of the current and voltage.

21. (Withdrawn) The method of claim 17, wherein varying at least one of the current and voltage further comprises varying the magnitude of at least one of the current and voltage.

22. (Previously Presented) A system, comprising:

means for forming a first dielectric layer above a first structure layer;

means for forming a first opening in the first dielectric layer;

means for forming a first copper layer above the first dielectric layer and in the first opening;

means for measuring an actual thickness of the copper layer, measuring the actual thickness comprises averaging a plurality of thicknesses from a plurality of locations on said first copper layer;

means for comparing the actual thickness to a desired thickness;

means for measuring a mechanical stress relating to said first copper layer;

means for varying at least one parameter used to form the first copper layer in response to the actual thickness differing from the desired thickness and said mechanical stress.

23. (Withdrawn) A system, comprising:

an electroplate tool capable of depositing a layer of copper above a surface of a semiconductor device, said electroplate tool having at least one parameter that may be varied to control a thickness of the layer of copper;

a metrology tool capable of measuring the thickness of the copper layer and delivering a signal indicative thereof; and

a controller adapted for receiving the signal, comparing the measured thickness to a desired thickness, and varying the at least one parameter in response to the measured thickness differing from the desired thickness.

24. (Withdrawn) The system of claim 23, wherein the controller varying the at least one parameter further comprises the controller varying an amount of time that the first copper layer is electroplated above the surface of the semiconductor device.

25. (Withdrawn) The system of claim 24, wherein the controller further comprises the controller being adapted for increasing the amount of time that the first copper layer is electroplated above the surface of the semiconductor device in response to the desired thickness being greater than the actual thickness.

26. (Withdrawn) The system of claim 24, wherein the controller further comprises the controller being adapted for decreasing the amount of time that the first copper layer is electroplated above the surface of the semiconductor device in response to the desired thickness being less than the actual thickness.

27. (Withdrawn) The system of claim 23, wherein the controller further comprises the controller being adapted for varying at least one of a current and voltage applied to an anode of the electroplate tool while electroplating the layer of copper above the surface of the semiconductor device.

28. (Withdrawn) The system of claim 27, wherein the controller further comprises the controller being adapted for increasing at least one of the current and voltage while the first copper layer is electroplated above the surface of the semiconductor device in response to the desired thickness being greater than the actual thickness.

29. (Withdrawn) The system of claim 27, wherein the controller comprises the controller being adapted for decreasing at least one of the current and voltage while the first copper layer is electroplated above the surface of the semiconductor device in response to the desired thickness being less than the actual thickness.

30. (Withdrawn) The system of claim 27, wherein the controller further comprises the controller being adapted for varying the frequency of at least one of the current and voltage.

31. (Withdrawn) The system of claim 27, wherein the controller further comprises the controller being adapted for varying the magnitude of at least one of the current and voltage.